AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0030] with the following amended paragraph:

[0030] Fig.6 shows the parasitic diode 62 formed by the switch element 52 in the off position in Fig.5. The parasitic diode 62 acts as a varactor 63 connected between node A and the second oscillator node OSC_N. The varactor 63 has a parasitic capacitance of Cp determined by the voltage ~~Va~~ V_A at node A in Fig.5.

Please replace paragraph [0031] with the following amended paragraph:

[0031] Fig.7 shows a capacitance vs. reverse voltage diagram of the varactor 63 shown in Fig.6. As the reverse voltage ~~(Va)~~ $(-V_A)$ across the varactor 63 changes, the associated parasitic capacitance Cp changes. However, this change is not linear. Reverse voltages within the threshold voltage ~~Vt~~ V_{th} of the first switch element 52 have the greatest parasitic capacitance Cp changes. The present invention uses this fact to precharge node A to a voltage much larger than the threshold voltage of the switch element 52 (VDD for example). This means that as the charge on node A leaks to ground through the first switch element 32, the parasitic capacitance remains approximately the same because. In this way, the locking period of the VCO is shortened and the present invention allows the frequency synthesizer to reach a stable state

faster than the prior art implementations.

Please replace paragraph [0032] with the following amended paragraph:

[0032] Fig.8 shows a time domain plot of the first control signal SW1, the second control signal SW2, and the voltage at node A in Fig.5. To switch the switched capacitor circuit 20d to an off state, at time t1 the first control signal SW1 drops to a logic low. This causes the first switch element 52 to switch off, disconnecting node A from ground. At the same time, the precharge switch element 56 is turned on, connecting node A to the power supply node VDD through the second switch element 58. The voltage ~~Va~~ V_A at node A ramps up toward the precharge voltage, which in this embodiment is VDD. The delay unit 60 delays the first control signal SW1 by a predetermined delay period TDELAY to create the second control signal SW2, which shuts off the second switch element 58 after the predetermined delay period TDELAY. When the second switch element 58 shuts off, node A is disconnected from the precharge voltage VDD. There will be a gradual drop in the voltage ~~Va~~ V_A at node A after t2 due to leakage currents through the first switch element 52 to ground, however, as the varactor 63 formed by the parasitic diode 62 of the first switch element 32 in the off state is predominately affected by reverse voltages close to the threshold voltage, there will be only a slight capacitance Cp difference. At time t3, the switched capacitor circuit 20d is turned back on by the first control signal SW1 returning to a logic

high level. The precharge switch element 56 is turned off and the first switch element 52 is turned on, reconnecting node A to ground.

Please replace paragraph [0035] with the following amended paragraph:

[0035] Fig.10 shows a time domain plot of the first control signal SW1, the second control signal SW2, the voltage ~~Va~~ V_A at node A, and the voltage ~~Vb~~ V_B at node B in Fig.9. To switch the switched capacitor circuit 20e to an off state, at time t1 the first control signal SW1 drops to a logic low. This causes the first positive side switch element 74 and the first negative side switch element 76 to switch off, disconnecting from ground node A and node B respectively. At the same time, the precharge switch element 80 is turned on, connecting node A and node B to a precharge voltage, which is a power supply voltage VDD. The voltages at node A ~~(Va)~~ (V_A) and node B ~~(Vb)~~ (V_B) ramp up toward VDD as the parasitic capacitance of the varactors formed by the first positive and negative side switch elements 74, 76 are charged by the precharge circuit 78. The delay unit 86 low-pass filters the first control signal SW1 to create the second control signal SW2, which shuts off the second switch element 58 after a predetermined delay period TDELAY. The predetermined delay period TDELAY is defined by how long the second control signal SW2 takes to cross a threshold line causing the second positive and negative switch elements to shut off. When the second positive and negative side switch elements 74, 76 shut off, node

A and node B are disconnected from the precharge voltage VDD. There will be a gradual drop in the voltage ~~Va~~ V_A at node A and in the voltage ~~Vb~~ V_B at node B due to leakage currents to ground through the first positive and negative side switch elements 74, 76. However, as the varactors 63 formed by the parasitic diode 62 of the first positive side switch element 74 and the first negative side switch element 76 in the off state are predominately affected by reverse voltages close to the threshold voltage, there will be only a slight capacitance Cp difference. At time t3, the switched capacitor circuit 20e is turned back on by the first control signal SW1 returning to a logic high level. The precharge switch element 80 is turned off and the first positive and negative side switch elements 74, 76 are turned on, reconnecting nodes A and B to ground.

Please replace paragraph [0036] with the following amended paragraph:

[0036] Fig.11 shows a differential switched capacitor circuit according to the third embodiment of the present invention. The third embodiment differential switched capacitor circuit 20f comprises the same basic components as the second embodiment shown in Fig.9. However, in the third embodiment, the precharge circuit 78 further comprises a third positive side switch element 100 and a third negative side switch element 102. In time division multiple access (TDMA) based radio systems, the actual transmission time for each time-slot is limited to a TDMA time period

typically around 400us. Because of this short TDMA time period, the gradual leakage of the charge at node A and node B is not a concern. The varactors 63 formed by the first positive and negative side switch elements are always reverse biased with a large voltage, and therefore there is very little difference in the parasitic capacitance Cp of the varactors 63 over the TDMA time period. However, in ~~carrier sense~~ code division multiple access (CDMA) based radio systems, the VCO needs to continuously function. In this situation, the gradual leakage of the voltage at node A and node B needs to be prevented. In the third embodiment of the present invention, the third positive and negative side switch elements 100, 102 prevent this gradual leakage of charge from nodes A and B.

Please replace paragraph [0038] with the following amended paragraph:

[0038] Fig.12 shows a time domain plot of the first control signal SW1, the second control signal SW2, the voltage ~~Va~~ V_A at node A, and the voltage ~~Vb~~ V_B at node B in Fig.11. The first control signal SW1 and the second control signal SW2 switch off the differential switched capacitor circuit 20f at time t1, similar to the second embodiment shown in Fig.10. However using the third embodiment shown in Fig.12, due to the addition of the third positive side switch element 100 and the third negative side switch element 102, there is no gradual drop in the voltage ~~Va~~ V_A at node A or in the voltage ~~Vb~~ V_B at node B. The third embodiment

differential switched capacitor circuit 20f shown in Fig.11 prevents frequency drift of the VCO due to gradual leakage of node A and node B to ground through the first positive and negative side switch elements 74, 76 in the off-state and is suitable for CDMA based systems.